





1

# The Future of ASIC Design(ers)

Steve Golson Trilobyte Systems

Phone: +1.978.369.9669 Email: sgolson@trilobyte.com Web: http://www.trilobyte.com





## The ASIC Designer's Lament

• How did I get here?

• Who did this to me?

• What will happen next?



Δ



## 1968 -- The beginning

- Hand-drawn schematics
- Standard cells -- new library for each product line ~6 kinds of gates, ~4-5 speed ranges
- Gate sizing by hand using CT curves (load vs. delay)
- Place & route by hand on mylar
- TTL breadboard for verification
- Transistor-level timing analysis using SPICE-like programs

Designer thinks about: Gates, transistors, breadboard, and maybe library





## Early 1970s -- some improvements

- + Module-level design (multiple designers working on one chip)
- + Software simulation (cycle-based)
- + On-chip bus design (trade wires for time)
- + Pitch-matched layout (datapath, PLA, ROM, RAM)
- + MOS-specific circuit techniques (dynamic logic)

Designer thinks about: Gates, netlist simulation, floorplan, transistors







## Early 1980s -- LSI Logic et al.

- Hand-drawn schematics
- Hand-typed netlist
- + Automatic place and route
- Netlist simulation
- + Gate-level timing analysis

Designer thinks about: Gates, netlist simulation



### Mid 1980s -- some improvements

- + Schematic capture
- + Automatic netlist generation
- Automatic place and route
- Netlist simulation
- Gate-level timing analysis

Designer thinks about: Gates, netlist simulation



## Early 1990s -- Verilog and synthesis

- + RTL Verilog
- + RTL simulation
- + Synthesized netlist
- Netlist simulation
- Automatic (?) place and route
- Gate-level timing analysis

Designer thinks about: RTL code, RTL simulation, gates, netlist simulation





- Q: When it was introduced by Gateway in 1985, Verilog was marketed as what sort of simulator?
- A: Verilog was introduced as the ultimate mixed-mode simulator, capable of simulating digital systems at the register transfer *and* gate levels

Multiple levels of abstraction!



## Late 1990s -- Behavioral synthesis

- + Behavioral Verilog, some generated by graphical HLDA tools
- + Behavioral Verilog and HLDA simulation
- RTL Verilog, some automatically generated by HLDA tool
- RTL simulation
- Synthesized netlist
- Netlist simulation
- Automatic (???) place and route
- Gate-level timing analysis
- + FPGA breadboard



### Late 1990s -- Behavioral synthesis

Designer thinks about: Behavioral code, RTL code, gates, floorplan, behavioral simulation, RTL simulation, netlist simulation, breadboard



## 2001 and beyond the infinite...

- + System design language (C++, Superlog, SystemC, etc.)
- + System design language simulation and formal verification
- + System design language synthesis
- RTL Verilog
- RTL simulation
- Floorplan
- RTL synthesized netlist & placement (physical synthesis)
- Netlist simulation
- Gate-level timing analysis



### 2001 and beyond the infinite...

Designer thinks about: System code, RTL code, gates, floorplan, placement, system simulation, formal verification, RTL simulation, netlist simulation, breadboard









### Top Ten EDA Companies ranked by 2001 revenues (\$M)

Cadence	\$1,430	
Synopsys	\$700	
Mentor Graphics	\$600	
Avant!	\$399	
	Cadence Synopsys Mentor Graphics Avant!	Cadence\$1,430Synopsys\$700Mentor Graphics\$600Avant!\$399



### Top Ten EDA Companies ranked by 2001 revenues (\$M)

1.	Cadence	\$1,430
2.	Synopsys	\$700
3.	Mentor Graphics	\$600
4.	Avant!	\$399
5.	Innoveda	\$91
6.	IKOS	\$55
7.	Simplex	\$50
8.	Synplicity	\$49
9.	Verisity	\$39
10.	Magma	\$35



## Top Ten EDA Companies

by 2001 revenues with current market capitalization

		Revenues \$M	Market cap \$M
1.	Cadence	\$1,430	\$5,477
2.	Synopsys	\$700	\$3,183
3.	Mentor Graphics	\$600	\$1,615
4.	Avant!	\$399	\$724
5.	Innoveda	\$91	\$86
6.	IKOS	\$55	\$107
7.	Simplex	\$50	\$132
8.	Synplicity	\$49	\$202
9.	Verisity	\$39	\$363
10.	Magma	\$35	\$575

Market capitalization from Yahoo Finance as of 5 March 2002



### **Provocative Postulate**

#### All innovation in EDA comes from startups.





### **Provocative** Polite Postulate

Postulate

Almost all innovation in EDA comes from startups.

Corollary

Some EDA innovation comes from established companies acting like startups.



### **Provocative** Polite Postulate

Postulate

Almost all innovation in EDA comes from startups.

Corollary #1

Some EDA innovation comes from established companies acting like startups.

Corollary #2

Some EDA innovation comes from established companies who have been provoked by pesky startups that threaten to eat their lunch.



Q: What was the first software company to go public?

Q: What year was it?

Q: How much did they raise in their IPO?

Q: What provided a significant part of their income?



- Q: What was the first software company to go public?
- A: Cullinane Corporation (NYSE)
- Q: What year was it?
- A: 1968
- Q: How much did they raise in their IPO?
- A: \$500,000
- Q: What provided a significant part of their income?
- A: They charged 10% of their initial license fee in mandatory annual support.





Q: How do EDA companies set their prices? How do they decide what to charge?

A: Prices are set relative to existing products already in the marketplace.



## The Black Art of EDA Pricing

"...the first substantial entrant gets to price on it's product's absolute value to the customer.

The followers then price their products based on their value relative to the first supplier's."

William H. Davidow, Marketing High Technology



## The Black Art of EDA Pricing M&A

"...the first substantial entrant gets to price on it's product's absolute value to the customer.

The followers then price their products based on their value relative to the first supplier's.

As long as the market contains relatively few competitors, the products are likely to maintain this type of price relationship."

William H. Davidow, Marketing High Technology



### Points to Ponder

- What motivates an EDA company to introduce a new product?
- What motivates an EDA company executive?
- What motivates an EDA company manager?
- What motivates an EDA company R&D engineer?

Do any of these people design chips?







- Perhaps for some vendors, and not for others
- Captive EDA tools may make a comeback
- EDA tools finally get a chance to catch up with fab technology
- We get to do real engineering again

It's way way off in the far distant future, anyway.

lsn't it?



### That's all, folks!

Any questions?